REMARKS/ARGUMENTS

Claims 1-27 are pending in the present application. In the Office Action mailed April 17, 2006, the Examiner rejected claims 1-27 under 35 U.S.C. § 102.

Claim 1 is amended to correlate the assertion of the data read/write commands to the memory testing program specific to the first memory block. Support can be found in Paragraph [0039], lines 5-7. No new matter is introduced.

Reconsideration is respectfully requested in view of the above amendments to the claims and the following remarks.

A. Specification

The abstract is amended to remove the expression "is provided" to overcome the examiner's objection, and no new matter is introduced.

B. Claim Objections

The claims are amended to provide sufficient line indentation to overcome the examiner's objection.

C. Claims 1-27 Rejected Under 35 U.S.C. § 102(b)

The Office Action rejected claims 1-27 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,421,798 to Lin et al. (hereinafter, "Lin"). This rejection is respectfully traversed.

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." MPEP § 2131 (citing Verdegaal Bros. v. Union Oil Co. of California, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987)). "The identical invention must be shown in as complete detail as is contained in the ... claim." Id. (citing Richardson v. Suzuki Motor Co., 9 USPQ2d 1913, 1920 (Fed. Cir. 1989)). In addition, "the reference must be enabling and describe the applicant's claimed invention sufficiently to have placed

it in possession of a person of ordinary skill in the field of the invention." In re Paulsen, 31 USPQ2d 1671, 1673 (Fed. Cir. 1994).

Applicant respectfully submits that the claims at issue are patentably distinct from Lin. Lin does not disclose all of the limitations in the claims.

Claims 1-14

According to Page 3 of the Office Action regarding independent claim 1, Lin's main memory 108, address space 412, address space 424, CPU 102, BIOS 104 and host bridge 304 are cited by the examiner to be equivalent to the memory control module, first memory block, second memory block, processing unit, means for providing memory test program to be executed by the processing unit, and control chip of the present invention. The Applicant respectfully traverses examiner's citations.

Please refer to Fig. 4 and the relevant descriptions, Lin's address spaces 412 and 424 are two examples of the address space 400, wherein the address space 412 is used in conventional systems while the address space 424 is applied to a disclosed embodiment (col. 4, lines 64-66). In other words, the address spaces 412 and 424 are not two blocks included in a memory control module. Furthermore, each of the address spaces 412 and 424 are provided with a main memory address space, a PCI address space and an upper address space including a BIOS address space (col. 5, line 27 ~ col. 6, line 23). Some of the sections of the address space 412 or 424 are associated with the memory 108, but some do not. For example, the main memory address space 414 is associated with the physical memory 108 (col. 5, lines 57-62) while the PCI address space 428 where the high-speed BIOS code is stored is not associated with the address space of physical memory 108 (col. 6, lines 30-32). Accordingly, neither of the address spaces 412 and 424 could be comprised by the main memory 108, as the first and second memory blocks are comprised by the memory control module in the present invention.

Furthermore, Lin fails to disclose or suggest that a second memory block is accessed for test in response to a certain state of read/write commands asserted by executing a memory test program specific to a first memory block. On the other hand, Lin's BIOS code considered to be equivalent to

the memory test program by the examiner is supposed to be applied to any memory seated in memory socket 110.

As a matter of fact, Lin offers a method of testing memory in a personal computer, replacing that tested memory with new untested memory, and then testing the new untested memory while the PC is operational (col. 2, lines 54-58). The method is applicable to any size of physical memory space provided the chipset 100 and CPU 102 can accommodate such as addressable space (col. 5, lines 1-11). It is thus inherent that according to Lin, each test is performed for the entire memory instead of testing a part of the memory in a state and testing another part of the memory in another state. In other words, the chipset 100 and CPU 102 have to be modified if the memory is changed from four-gigabyte to eight-gigabyte.

In view of the foregoing, claim 1 is not anticipated by Lin. Claim 1 and claims 2-13 dependent on claim 1 should be patentable.

Claims 14-16

Similar discussion on claim 1 can be applied to claim 14. Lin fails to disclose or suggest testing different memory blocks of a memory control module at different time points with read/write commands for testing one of the memory blocks. Thus claim 14 is not anticipated by Lin. Claim 14 and claims 15-16 dependent on claim 14 should be patentable.

Claims 17-27

Similar discussion on claim 1 can be applied to claim 17. Furthermore, Lin fails to disclose or suggest dividing a memory control module into at least a first memory block and a second memory block that respond to data read/write commands asserted in different situations. Lin's address spaces 412 and 424 cited to be equivalent to the first and second memory blocks by the examiner are separate instead of divisions of a memory control module. Thus claim 17 is not anticipated by Lin. Claim 17 and claims 18-27 dependent on claim 17 should be patentable.

C. Conclusion

Applicant respectfully asserts that all pending claims 1-27 are patentably distinct from the cited references, and request that a timely Notice of Allowance be issued in this case. If there are any remaining issues preventing allowance of the pending claims that may be clarified by telephone, the Examiner is requested to call the undersigned.

Respectfully submitted,

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